REMARKS

The above-referenced application has been reviewed in light of the Examiner's Final Office Action dated December 15, 2004. Claim 23 has been canceled, and Claims 1, 14 and 24 have been amended. Accordingly, Claims 1-22 and 24 are currently pending in this application. These amendments are supported by the specification as originally filed, and no new matter has been added. The Examiner's reconsideration of the rejections in view of the above amendments and the following remarks is respectfully requested.

In accordance with the Office Action, the Examiner has indicated that the Japanese patent reference JP62063344 is not in the file (*see* O.A. at 2, para. 3). The Japanese patent reference JP62063344 was previously provided with Paper No. 4 on July 23, 2002. Accordingly, a replacement copy of the reference and a new English abstract are provided herewith for the Examiner's convenience. If the Examiner requires anything further to facilitate consideration of this reference, the Examiner is encouraged to contact Applicants' undersigned attorney at the number indicated below.

In accordance with the Office Action, a replacement Abstract of the Disclosure drew an objection for failure to start on a separate page in accordance with 37 CFR § 1.52(b)(4) (*see* O.A. at 2, para. 4). An amended Abstract is provided herewith, beginning on a separate page.

In accordance with the Office Action, Claims 1-7, 14-16, 21, and 23-24 stand rejected under 37 USC § 103(a) as being obvious over U.S. Patent No. 4,715,013 to MacGregor et al. in view of U.S. Patent No. 5,579,493 to Kiuchi et al. Applicant

respectfully traverses with respect to Claim 23, now canceled, subject matter of which has been incorporated into amended Claims 1, 14 and 24. Amended Claims 1, 14 and 24 have been changed to correct minor errors of a generally typographical nature and to recite subject matter from the former Claim 23. No new matter has been added, and more particularly, no new issues have been raised.

The '715 patent to MacGregor et al. is generally directed towards a device having a processor and a coprocessor, and the use of a logical bus structure with the processors. Thus, MacGregor shows coprocessors but makes no teaching or suggestion of a loop buffer for processing loop instructions.

The '493 to Kiuchi et al. is generally directed towards a data processor for processing loop instructions. Thus, Kiuchi shows processing loop instructions, but makes no teaching or suggestion for the use of a coprocessor with the CPU in the context of processing loop instructions.

Original Claim 23, now canceled, recited, *inter alia,* "the instructions stored in the loop buffer comprise coprocessor and CPU type instructions." Applicants respectfully submit that even if, *arguendo,* one skilled in the art were to combine the CPU and coprocessor of MacGregor et al. with the CPU and loop instructions of Kiuchi et al., one would not achieve a "data processing device ... wherein the instructions stored in the loop buffer comprise coprocessor and CPU type instructions." At most, such combination would only achieve a device having a processor and a coprocessor where one, but not both, might process instructions from a single loop buffer. Thus, Kiuchi cannot cure the deficiencies of MacGregor with respect to the technical hurdles

necessary to achieve cooperative execution of both CPU-type and coprocessor-type instructions held in a single loop buffer, as both taught and claimed by the present Applicants.

Claim 1 has been amended to recite, *inter alia,* a "method of processing loop instructions using a data processing device having a central processing unit (CPU) and a coprocessor ... comprising ... executing at least one coprocessor-type instruction from the loop buffer by the coprocessor, and forwarding any CPU-type instructions from the loop buffer to the CPU for execution". Accordingly, the recitations of amended Claim 1 are neither taught nor suggested by '715 patent to MacGregor et al. in view of the '493 patent to Kiuchi et al.

Similarly, Claim 14 has been amended to recite, *inter alia,* a "data processing device ... wherein the loop buffer instructions of coprocessor-type are executed by the coprocessor and the loop buffer instructions of CPU-type are forwarded to the CPU for execution." Accordingly, the recitations of amended Claim 14 are neither taught nor suggested by the '715 patent in view of the '493 patent. Likewise, amended Claim 24 recites like limitations that are neither taught nor suggested by MacGregor in view of Kiuchi, nor by any of the other references of record in this case.

Conclusion

Accordingly, it is respectfully submitted that amended independent Claims 1, 14 and 24 are in condition for allowance for at least the reasons stated above. Since Claims 2-13 and 15-22 each depend from one of the above claims and necessarily include each of the elements and limitations thereof, it is respectfully submitted that these claims are also in condition for allowance for at least the reasons stated, and for reciting additional patentable subject matter. Thus, each of Claims 1-22 and 24 is in condition for allowance. All issues raised by the Examiner having been addressed, reconsideration of the rejections and an early and favorable allowance of this case is earnestly solicited.

Respectfully submitted,

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